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EXAMINER	
CHO, JAMES HYONCHOL	
ART UNIT	PAPER NUMBER
2819	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,601	KER ET AL.	
	Examiner	Art Unit	
	James Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-20,25-31,34 and 35* is/are rejected.

7)☒ Claim(s) *9,21-24,32,33 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-25-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claims 12, 14, 20-21, 23, 28 and 32 are objected to because of the following informalities:

In claim 12, "the source and drain of the fifth transistor" on lines 6-7 appears to be --a source and drain of a fifth transistor--;

In claim 14, "a tracking circuit" on line 15 appears to be --the tracking circuit--;

In claim 20, "the third PMOS transistor" on line 1 appears to be --a third PMOS transistor--;

In claim 21, "the second part" on line 1 appears to be --the second part of the tracking circuit--;

In claim 23, "the second part" on line 1 appears to be --the second part of the tracking circuit--;

In claim 28, "a tracking circuit" on line 6 appears to be --the tracking circuit--; and

In claim 32, "one of" on line appears to be --and one of--.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 14-20, 25-31 and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by Ajit et al. (US PAT No. 6,313,672).

Regarding claim 1, Fig. 5 of Ajit et al. teaches a buffer circuit in a mixed-voltage circuit operating in a power supply voltage, comprising: a node (130); a driver circuit (21 and 220) coupled to the node comprising at least a first PMOS transistor (M1) having a substrate, a drain, a source, and a parasitic diode (parasitic diode in PMOS transistor is inherent) between the drain and the substrate, the driver circuit having an on-state and an off-state; and a second PMOS transistor (M5) having a source and a drain, one of the source and drain of the second PMOS transistor being coupled to the substrate of the first PMOS transistor, where the second PMOS transistor is turned off when a first signal having a voltage level higher than the power supply voltage is provided on the node (M2 is on, gate of M1 and M5 is coupled to 130 which is a high voltage so that M1 and M5 is turned off; col. 4, lines 4, lines 57-66).

Regarding claim 2, Fig. 5 of Ajit et al. teaches the circuit of claim 1 , where a voltage at the substrate of the first PMOS transistor has a level substantially equal to that of the first signal when the first signal appears on the node (when M3 is on, 130 is coupled to NW).

Regarding claim 3, Fig. 5 of Ajit et al. teaches the circuit of claim 1, where the second PMOS transistor (M5) has a gate and a substrate, the gate of the second PMOS transistor being coupled to the gate of the first PMOS transistor (M1), the substrate of

the second PMOS transistor being coupled to the substrate of the first PMOS transistor, and the other of the drain and source of the second PMOS transistor being connectable to receive the power supply voltage (VDD).

Regarding claim 4, Fig. 5 of Ajit et al. teaches the circuit of claim 1, where the second PMOS transistor is turned on when the driver circuit operates in the on-state and a voltage at the node is approximately equal to the power supply voltage (M1 is turned on when gate of M1 is low where the gate of M5 coupled to the gate of M1, which makes M5 to be on when 130 is VDD).

Regarding claim 5, Fig. 5 of Ajit et al. teaches the circuit of claim 1, where the driver circuit further comprises two stacked NMOS transistors (M6, M7) serially coupled to the first PMOS transistor, all of the first PMOS transistor and the two stacked NMOS transistors being off when the driver circuit is in the off state (input mode or tri-state mode; col. 4, line 41 - col. 5, line 4), and one of the first PMOS transistor or both of the two stacked NMOS transistors being on when the driver circuit is in the on state (output mode; col. 5, lines 5-16).

Regarding claim 14, Fig. 4 of Ajit et al. teaches a buffer circuit connectable to receive a power supply voltage (VDD), comprising; a node (130); a driver circuit (210 and 220) coupled to the node comprising at least a first PMOS transistor (M1), the first PMOS transistor having a gate and a substrate (NW), the driver circuit having an on-

state and an off-state; a second PMOS transistor (M4) having a source and a drain, one of the source and drain of the second PMOS transistor being coupled to the substrate of the first PMOS transistor (NW), where the second PMOS transistor is turned off when a first signal having a voltage level higher than the power supply voltage appears at the node (the gate of M4 is coupled to 130, the voltage level higher than VDD, thereby M4 is turned off); a first part of a tracking circuit (M2, M3, M5) coupled to the gate of the first PMOS transistor (M5 and M2 is coupled to the gate of M1) to provide a first bias to the gate of the first PMOS transistor when the first signal appears at the node (when a high voltage appears at 130, the gate of M1 is biased to 130); and a second part of the tracking circuit (pre-driver circuit) coupled to the gate of the first PMOS transistor to provide a second bias to the gate of the first PMOS transistor when the driver circuit is in the off-state and a second signal having a voltage level no greater than the power supply voltage appears at the node (when the buffer is in the receiver mode, i.e. high impedance and the node 130 is a logic low, pre-driver circuit provides a second bias).

Regarding claim 15, Fig. 4 of Ajit et al. teaches the circuit of claim 14, where the driver circuit further comprises a pair of stacked NMOS transistors (M6 and M7) coupled to the first PMOS transistor.

Regarding claim 16, Fig. 4 of Ajit et al. teaches the circuit of claim 14, where the voltage at the substrate of the first PMOS transistor is approximately equal to the voltage level of the first signal when the first signal appears at the node (M1 is turned on

when gate of M1 is low where the gate of M5 coupled to the gate of M1, which makes M5 to be on when 130 is VDD).

Regarding claim 17, Fig. 4 of Ajit et al. teaches the circuit of claim 14, where the first bias has a voltage level approximately equal to the voltage level of the first signal (M1 is turned on when gate of M1 is low where the gate of M5 coupled to the gate of M1, which makes M5 to be on when 130 is VDD).

Regarding claim 18, Fig. 4 of Ajit et al. teaches the circuit of claim 14, where the second bias has a voltage level approximately equal to the power supply voltage (when the buffer in receive mode, i.e. high impedance mode, the predriver circuit outputs VDD to turn off M1).

Regarding claim 19, Fig. 4 of Ajit et al. teaches the circuit of claim 14, where the first pad comprises a third PMOS transistor (M2) having a gate, a source, a drain, and a substrate, the gate of the third PMOS transistor is connectable to receive the power supply voltage (VDD), one of the source and drain of the third PMOS transistor is coupled to the node (130), the other of the source and drain of the third PMOS transistor is coupled to the gate of the first PMOS transistor (the gate of M1), and the substrate (NW) of the third PMOS transistor is coupled to the substrate (NW) of the first PMOS transistor.

Regarding claim 20, Fig. 4 of Ajit et al. teaches the circuit of claim 14, where a third PMOS transistor (M3 is turn on when the voltage at 130 is higher than VDD) is turned on when the first signal appears at the node.

Regarding claim 25, Figs. 1 and 4 of Ajit et al. teaches a system having a plurality of components operating at different voltage levels, comprising: a first chip (Fig. 1) including a first circuit; a second chip including a second circuit (col. 1, lines 50-53; buffer circuit operating at 3.3V and other circuit operating at 5V); a buffer circuit (Fig. 4) on the first chip having a receive mode and a transmit mode of operation (input/output mode determined by OE) and coupled between the first circuit and the second circuit, where the buffer circuit is connectable to a first power supply voltage (VDD) and the second circuit (other circuit; col. 1, lines 50-53) is connectable to a second power supply voltage (5V); a node (I/O node 130) coupling the buffer circuit to the second circuit; and a control signal terminal (OE terminal) for providing a first control signal (output mode when OE is a logic high) to switch the buffer circuit into the transmit mode, in which the buffer circuit receives at least one signal from the first circuit and outputs at least one signal to the second circuit, and for providing a second control signal (input mode when OE is a logic low) to switch the buffer circuit into the receive mode, in which the buffer circuit receives at least one signal from the second circuit and outputs at least one signal to the first circuit, where the buffer circuit comprises at least a driver circuit (M1).

Regarding claim 26, Figs. 1 and 4 of Ajit et al. teaches the system of claim 25, where the driver circuit comprises at least a first PMOS transistor (M1) having a drain and a substrate.

Regarding claim 27, Figs. 1 and 4 of Ajit et al. teaches the system of claim 26, where the buffer circuit further comprises a second PMOS transistor (M4) having a source and a drain, one of the source and drain of the second PMOS transistor being coupled to the substrate (NW) of the first PMOS transistor, where the second PMOS transistor is turned off when a first signal having a voltage level higher than the power supply voltage appears at the node (when 130 which is the gate of M4 is greater than VDD which is the source of M4, M4 is turned off).

Regarding claim 28, Figs. 1 and 4 of Ajit et al. teaches the system of claim 27, where the buffer circuit further comprises, a first part of a tracking circuit (M2, M3, M5) coupled to the gate of the first PMOS transistor to provide a first bias to the gate of the first PMOS transistor when the first signal appears at the node, where the first bias has a voltage level approximately equal to the voltage level of the first signal (when a high voltage appears at 130, the gate of M1 is biased to 130 since M2 is turned on), and a second part of a tracking circuit (pre-driver circuit) coupled to the gate of the first PMOS transistor to provide a second bias to the gate of the first PMOS transistor when a second signal having a voltage level lower than the first power supply voltage appears at the node, where the second bias has a voltage level approximately equal to the first

power supply voltage in the receive mode (when the buffer is in the receiver mode, i.e. high impedance and the node 130 is a logic low, pre-driver circuit provides a second bias).

Regarding claim 29, Figs. 1 and 4 of Ajit et al. teaches the system of claim 25, where the first power supply voltage is lower than the second power supply voltage (VDD=3.3 volts and the other circuit is operating at 5 volts).

Regarding claim 30, Figs. 1 and 4 of Ajit et al. teaches the system of claim 25, where the driver circuit is turned on in the transmit mode and turned off in the receive mode (in output mode, M1 is turned on when outputting an input signal of logic low while M1 is turned off in receive mode; col. 3, lines 41-45).

Regarding claim 31, Figs. 1 and 4 of Ajit et al. teaches the system of claim 28, where the first part of the tracking circuit comprises a third PMOS transistor (M2) having a gate, a source, a drain, and a substrate, and where the gate of the third PMOS transistor is connectable to the first power supply voltage (VDD), one of the source and drain of the third PMOS transistor is coupled to the node (130), the other of the source and the drain of the third PMOS transistor is coupled to the gate of the first PMOS transistor (gate of M1), and the substrate (NW) of the third PMOS transistor is coupled to the substrate (NW) of the first PMOS transistor.

Regarding claim 34, Figs. 1 and 4 of Ajit et al. teaches the system of claim 25, where the buffer circuit (Fig. 4 is the output stage of Fig. 1; col. 2, lines 64-67) further (see Fig. 1) comprises an input circuit (125 in Fig. 1) for receiving at least one signal from the second circuit and outputting at least one signal to the first circuit (input stage 125

Claims 6 - 8 and 10 - 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Morris et al. (US PAT No. 5,926,056).

Regarding claim 6, Fig. 2 of Morris et al. teaches a buffer circuit operable in a power supply voltage coupled between a first circuit having a first power level (0-3.3V) and a second circuit having a second power level (Fig. 3; 0-5 volts; col. 1, lines 9-34), comprising: a node (101); a driver circuit (103, 111, 112) comprising a first transistor (103) and a pair of stacked transistors (111,112), the first transistor having a gate, a source, and a drain, one of the source and the drain of the first transistor being coupled to the node, the stacked transistors comprising a second transistor (111) and a third transistor (112), a fourth transistor (109) having a source and a drain, one of the source and drain of the fourth transistor being coupled to the gate (107) of the first transistor, the other of the source and drain of the fourth transistor being coupled to the node, where the fourth transistor is turned on to provide a first bias to the gate of the first transistor when a first signal having a voltage level higher than the power supply voltage appears at the node (col. 2, line 33 - col. 3, line 17); and a gate-tracking circuit (104 and

105 , 108, 201, 202 coupled to 101 and 111 via 110 and coupled to 112 via 110 and 111) coupled to the node and the second and third transistors.

Regarding claim 7, Fig. 2 of Morris et al. teaches the circuit of claim 6 where the gate-tracking circuit comprises a fifth transistor (105) having a source, a drain, and a gate, one of the source and drain of the fifth transistor being coupled to the node (coupled 101 via 109), and the gate of the fifth transistor being coupled to both the second and third transistors (gate coupled to 111 and 112 via 110).

Regarding claim 8, Fig. 2 of Morris et al. teaches the circuit of claim 6 where the fourth transistor has a substrate coupled to the substrate of the first transistor (substrate of 109 Vf coupled to Vf of 103) and a gate (gate is coupled to VDD) connectable to receive the power supply voltage.

Regarding claim 10, Fig. 2 of Morris et al. teaches the circuit of claim 6, where the first bias has a voltage level approximately equal to that of the first signal (5v on 101 turns on 109, which provides 5v coupling to the gate of 103).

Regarding claim 11, Fig. 2 of Morris et al. teaches the circuit of claim 6, where the gate-tracking circuit further comprising a switch (104, 105; col. 1, lines 35-58), where the switch is turned on when the buffer circuit is in a transmit mode (in normal mode, 104 and 105 is on).

Regarding claim 12, Fig. 2 of Morris et al. teaches the circuit of claim 11, where the switch includes a sixth transistor (104) and a seventh transistor (105), each having a source, a drain, and a gate, one of the source and drain of the sixth transistor and one of the source and drain of the seventh transistor being coupled to the gate of the first transistor (104 and 105 is coupled to 107, the gate of 103), the gate of the sixth transistor being connectable to receive the power supply voltage (VDD), and the gate of the seventh transistor (105) being coupled to the other of the source and drain of the fifth transistor (110).

Regarding claim 13, Fig. 2 of Morris et al. teaches the circuit of claim 12, where the seventh transistor is turned on when a second signal having a voltage level lower than the power supply voltage appears at the node (when 0 volt is at 101, 110 and 109 are turned off and the seventh transistor 105 is turned on).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ajit et al. in view of Chow et al. (US PAT No. 6,060,906).

Regarding claim 35, Figs. 1 and 4 of Ajit et al. teaches the system of claim 34, where the input circuit discloses an input stage block, but does not disclose the details of the input circuit including an inverter and a third PMOS transistor. However, Fig. 2 of Chow et al. teaches a conventional bi-directional buffer circuit with an input buffer comprising an inverter 60, and a PMOS transistor (T5) used in different voltage level interface application for the purpose of reducing the stress voltage located at the input of the inverter 60 (col. 2, lines 26-29). Therefore, it would have been obvious at the time the invention was made to a person ordinary skill in the art to provide the input buffer circuit of Chow et al. in the place of the input stage block of Ajit et al. since it would provide protection from the stress voltage at the input inverter.

Allowable Subject Matter

Claims 9, 21-24, 32-33 and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Although Ajit et al. and Morris et al. teaches a buffer circuit that can tolerate over-voltage and Chow et al. teaches bi-directional buffer with specific details of the input stage, one of ordinary skill in the art would not have been motivated to modify the teaching of Ajit et al., Morris et al. and/or Chow et al. to further includes, among other things, the specific of the fifth transistor being turned on when the input signal appears at the node as recited in claim 9, the second part comprising a third PMOS transistor where the gate of the third PMOS transistor is coupled to both the first and second

NMOS transistors, one of the source and drain of the third PMOS transistor is coupled to the node as recited in claims 21 and 32 and the input terminal of the inverter coupled to both the first and second NMOS transistors of the buffer circuit as recited in claim 36.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Let et al. (US PAT No. 6,313,671) discloses a low-power integrated circuit I/O buffer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho
Primary Examiner
Art Unit 2819

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